

N- and P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	30	0.0355 at V _{GS} = 10 V	6.8	5.3
		0.0425 at V _{GS} = 4.5 V	6.2	
P-Channel	- 30	0.045 at V _{GS} = - 10 V	- 5.8	11.8
		0.062 at V _{GS} = - 4.5 V	- 5.0	

FEATURES

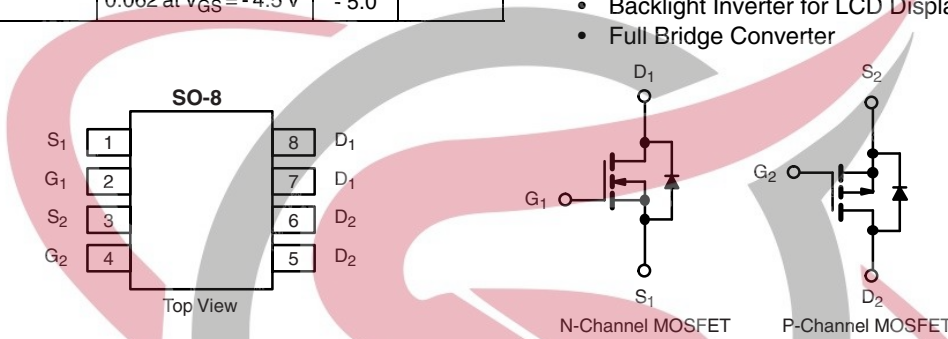
- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge Converter



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	30	- 30	V
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	6.8	- 5.8	A
	T _C = 70 °C	5.4	- 4.7	
	T _A = 25 °C	5.6 ^{b, c}	- 4.7 ^{b, c}	
	T _A = 70 °C	4.4 ^{b, c}	- 3.7 ^{b, c}	
Pulsed Drain Current	I _{DM}	20	- 20	A
Source-Drain Current Diode Current	T _C = 25 °C	2.5	- 2.5	
	T _A = 25 °C	1.6 ^{b, c}	- 1.6 ^{b, c}	
Pulsed Source-Drain Current	I _{SM}	20	- 20	A
Single Pulse Avalanche Current	I _{AS}	7	- 10	
Single Pulse Avalanche Energy	E _{AS}	2.45	5	mJ
Maximum Power Dissipation	T _C = 25 °C	3.0	3.1	W
	T _C = 70 °C	1.9	2	
	T _A = 25 °C	2.0 ^{b, c}	2.0 ^{b, c}	
	T _A = 70 °C	1.25 ^{b, c}	1.25 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	54	64	49	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	42	30	40	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 120 °C/W.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	30		V	
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-30			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\ \mu\text{A}$	N-Ch		44	mV/°C	
		$I_D = -250\ \mu\text{A}$	P-Ch		-42		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\ \mu\text{A}$	N-Ch		-5.5	mV/°C	
		$I_D = -250\ \mu\text{A}$	P-Ch		4.6		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	1.4		3.0	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-1.2		-2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA
			P-Ch			-100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	10			A
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		0.0295	0.0355	Ω
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		0.037	0.045	
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	N-Ch		0.0355	0.0425	
		$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	P-Ch		0.050	0.062	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$	N-Ch		22		S
		$V_{DS} = -15\text{ V}, I_D = -5\text{ A}$	P-Ch		14		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		640		pF
			P-Ch		970		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		73		pF
			P-Ch		120		
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		41		pF
			P-Ch		95		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch		11.7	20	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	P-Ch		25	38	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	N-Ch		5.3	9	nC
			P-Ch		11.8	18	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	N-Ch		1.9		nC
			P-Ch		3.0		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch	0.5	2.2	4.5	Ω
			P-Ch	1.0	5.5	11	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit		
Dynamic^a								
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}, R_L = 4\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch		7	14	ns	
Rise Time	t_r		P-Ch		7	14		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}, R_L = 4\ \Omega$ $I_D \cong -5\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	N-Ch		10	20		
			P-Ch		12	24		
Fall Time	t_f		N-Ch		15	30		
			P-Ch		30	60		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}, R_L = 4\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	N-Ch		16	30		
			P-Ch		44	80		
Rise Time	t_r		N-Ch		17	30		
			P-Ch		33	50		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}, R_L = 4\ \Omega$ $I_D \cong -5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\ \Omega$	N-Ch		16	30		
			P-Ch		28	60		
Fall Time	t_f		N-Ch		10	20		
			P-Ch		13	25		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			2.5		A
			P-Ch			-2.5		
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			20		
			P-Ch			-20		
Body Diode Voltage	V_{SD}	$I_S = 1.6\text{ A}$ $I_S = -1.6\text{ A}$	N-Ch		0.78	1.2	V	
			P-Ch		-0.76	-1.2		
Body Diode Reverse Recovery Time	t_{rr}		N-Ch		19	30	ns	
			P-Ch		26	50		
Body Diode Reverse Recovery Charge	Q_{rr}	N-Channel $I_F = 2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		14	25	nC	
			P-Ch		18.5	35		
Reverse Recovery Fall Time	t_a	P-Channel $I_F = -2\text{ A}, di/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		13		ns	
			P-Ch		12.5			
Reverse Recovery Rise Time	t_b		N-Ch		6			
			P-Ch		13.5			

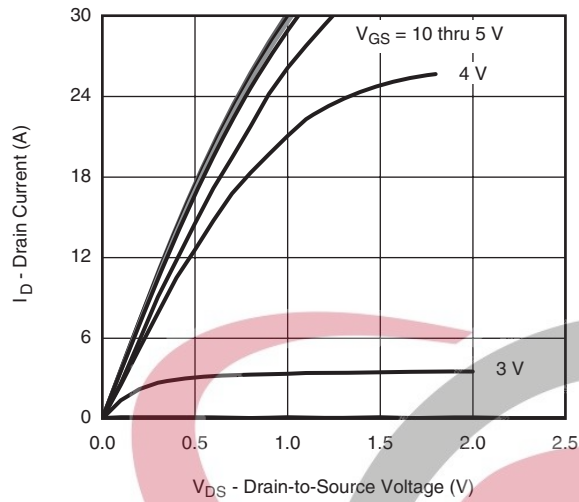
Notes:

a. Guaranteed by design, not subject to production testing.

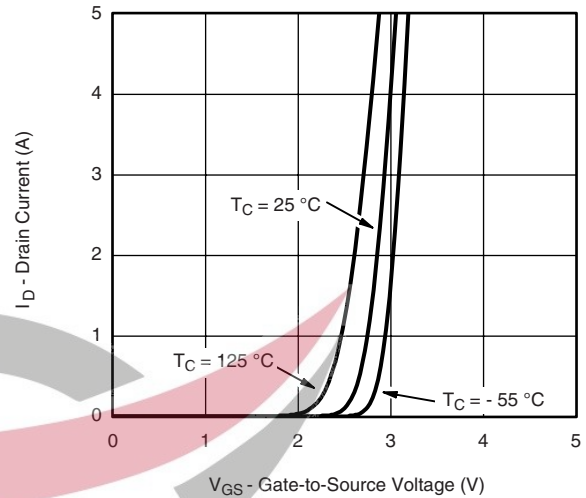
b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

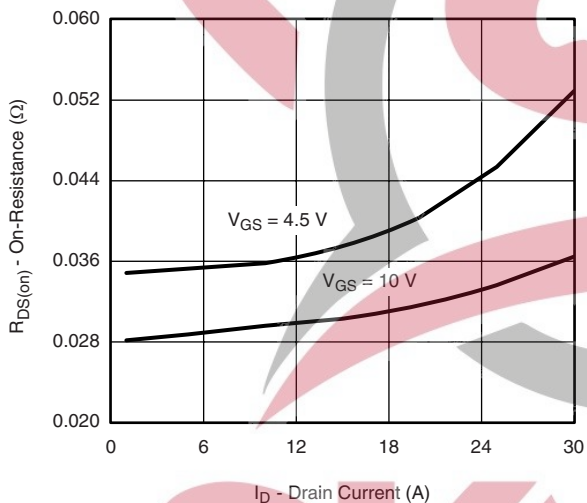
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



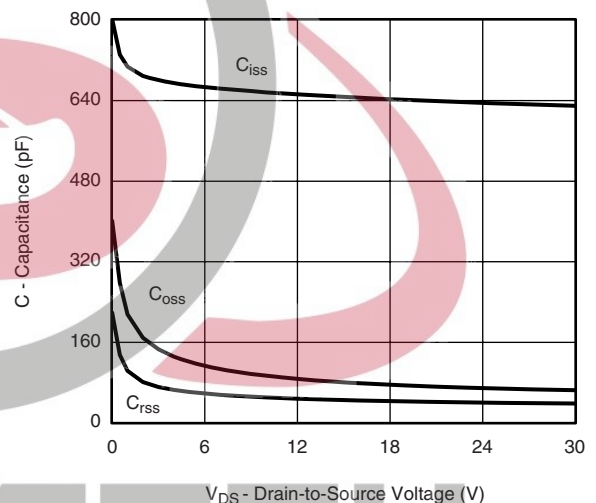
Output Characteristics



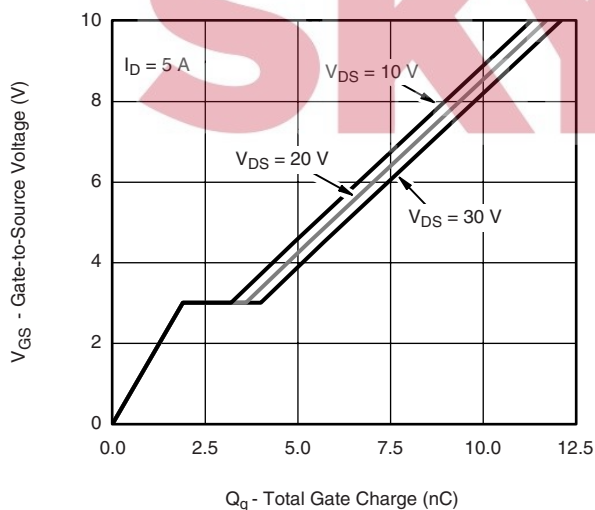
Transfer Characteristics



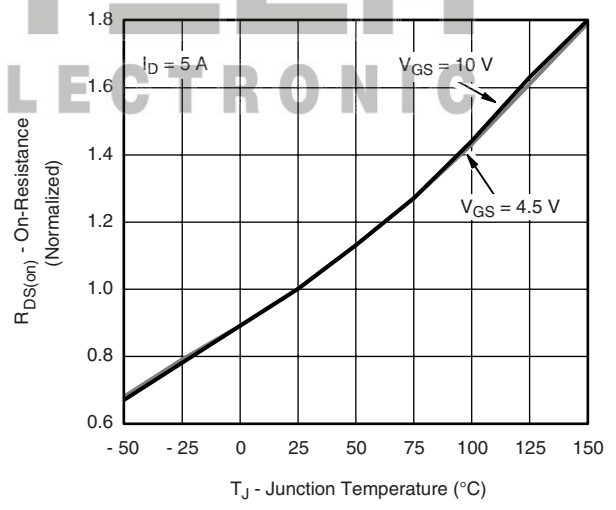
On-Resistance vs. Drain Current



Capacitance

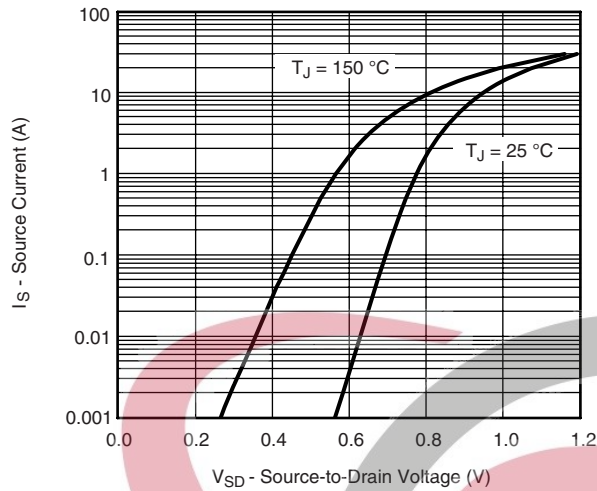


Gate Charge

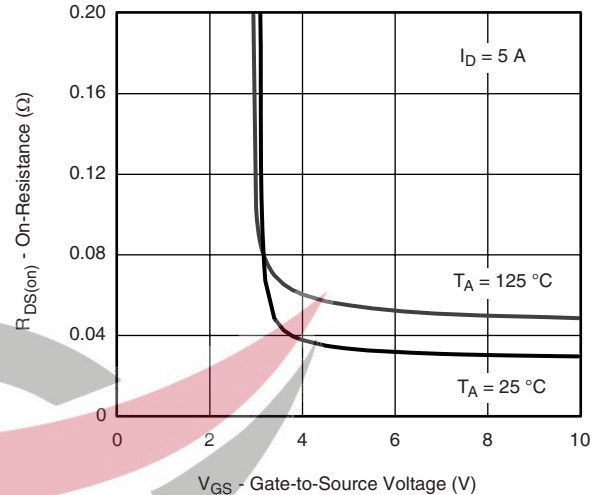


On-Resistance vs. Junction Temperature

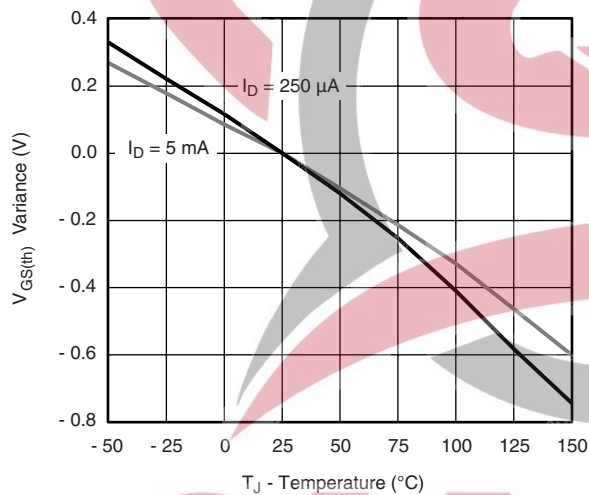
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



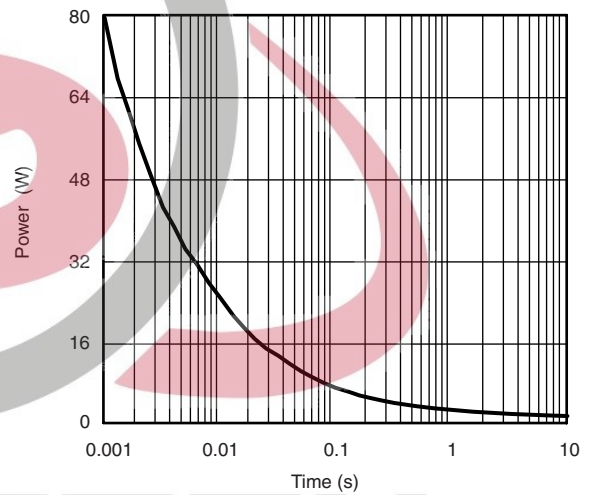
Source-Drain Diode Forward Voltage



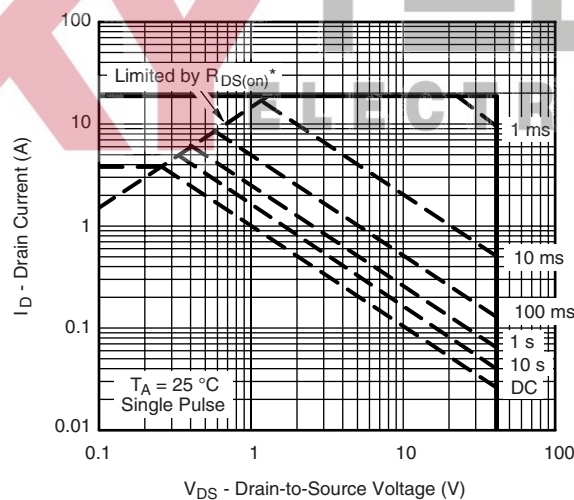
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



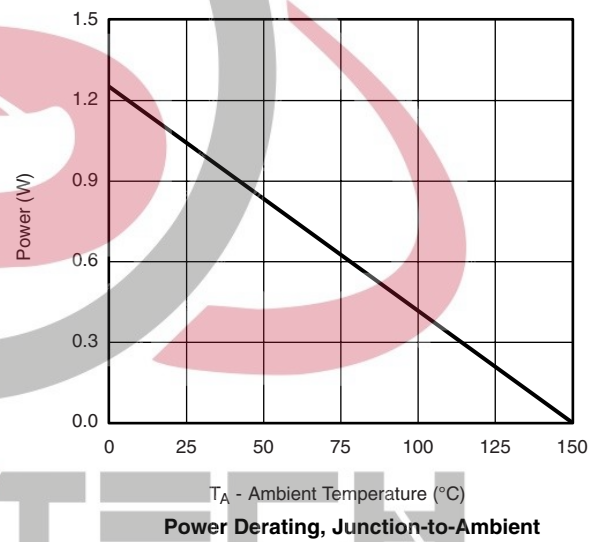
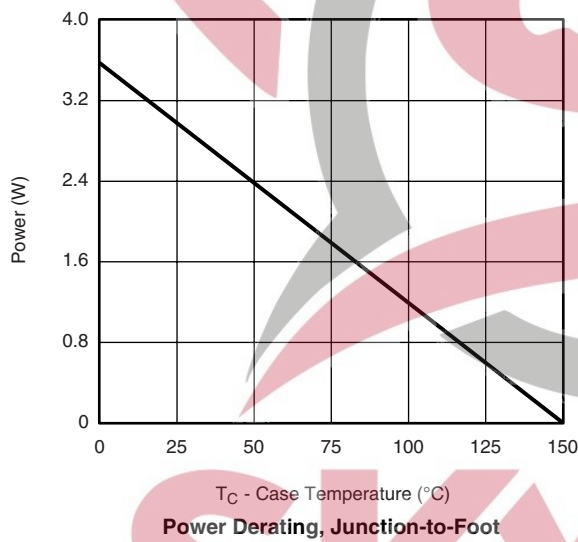
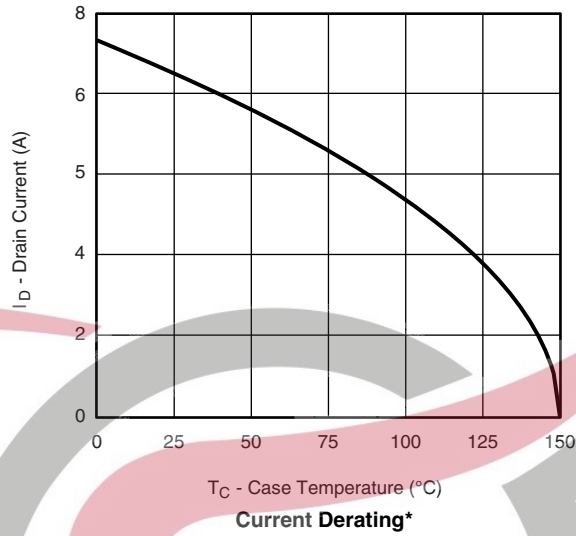
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

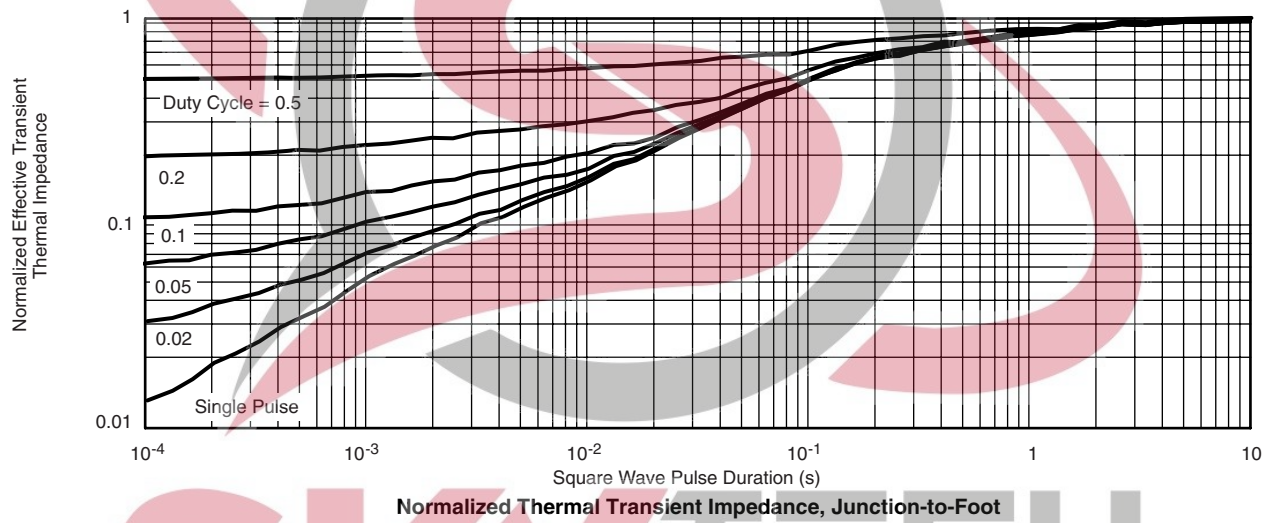
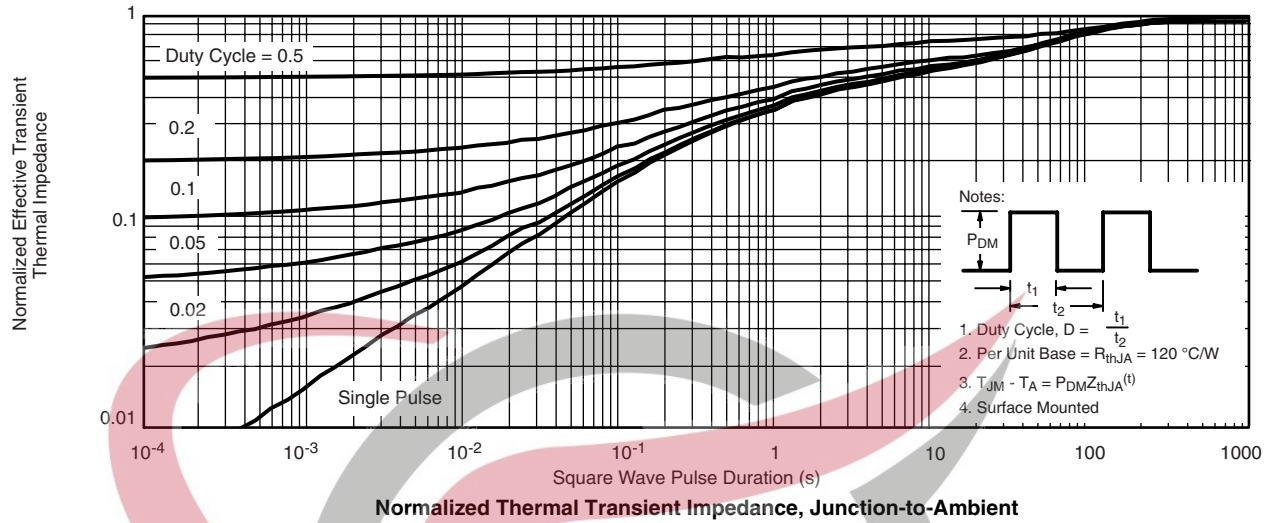
Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

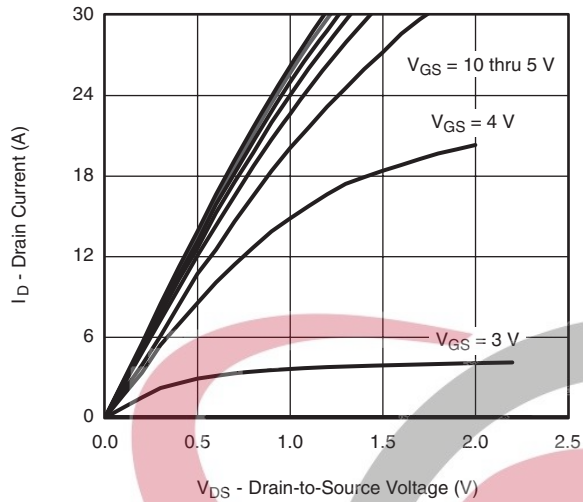


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

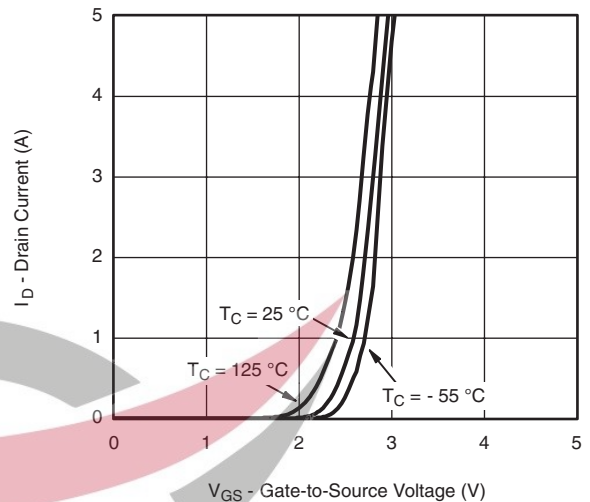
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



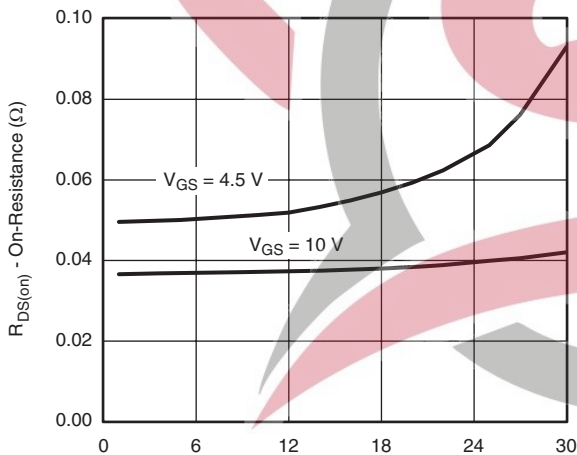
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



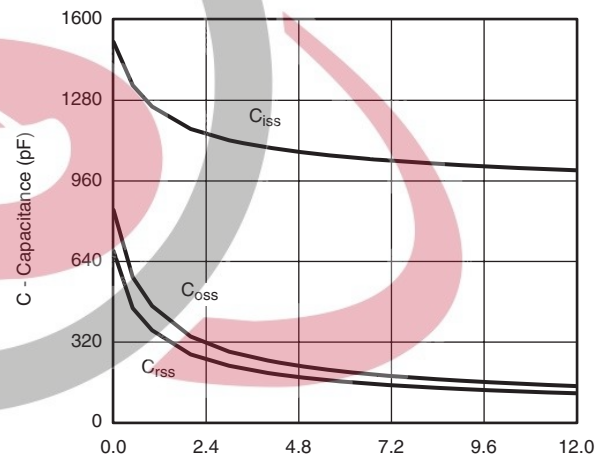
Output Characteristics



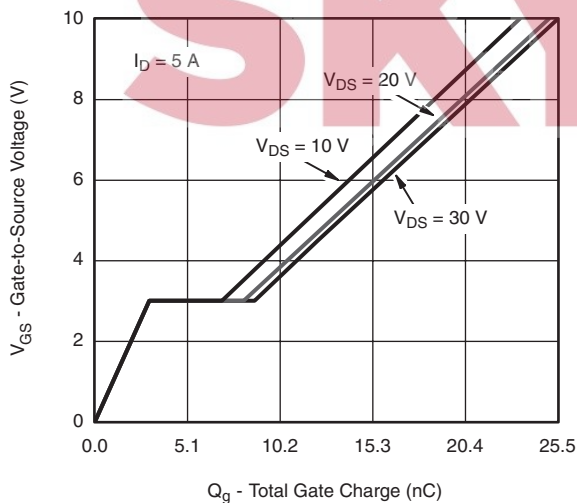
Transfer Characteristics



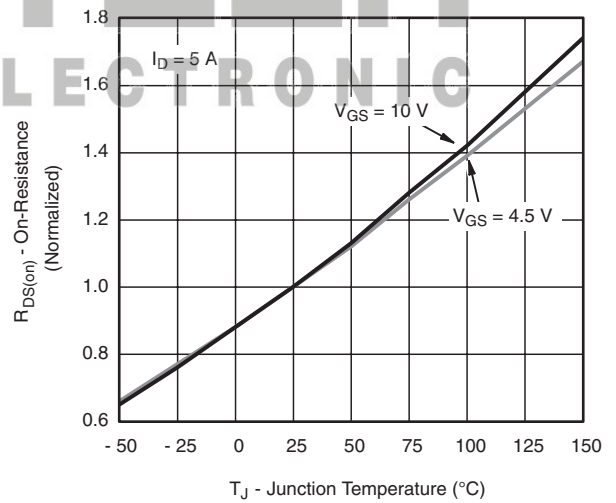
On-Resistance vs. Drain Current



Capacitance

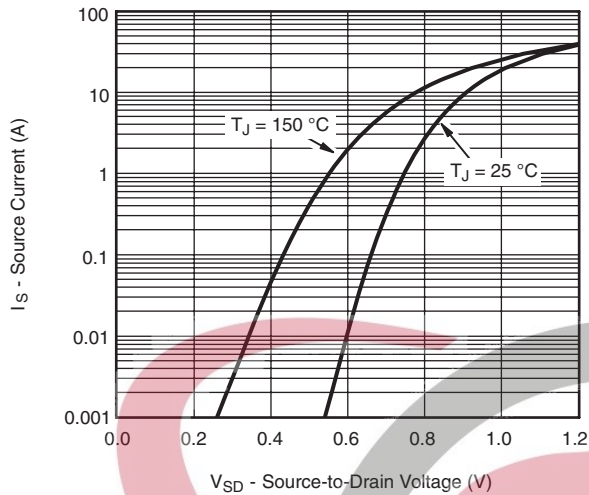


Gate Charge

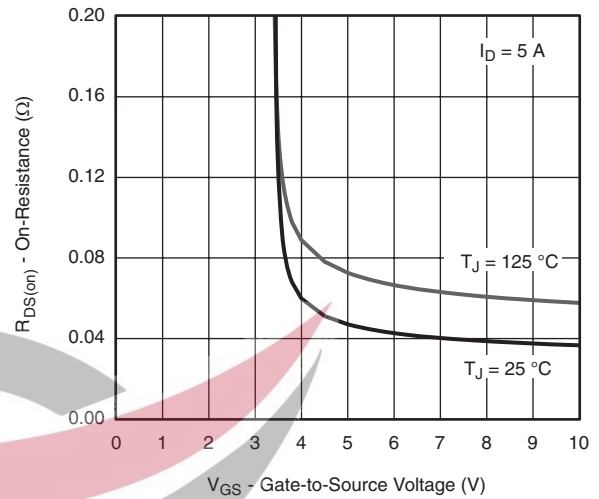


On-Resistance vs. Junction Temperature

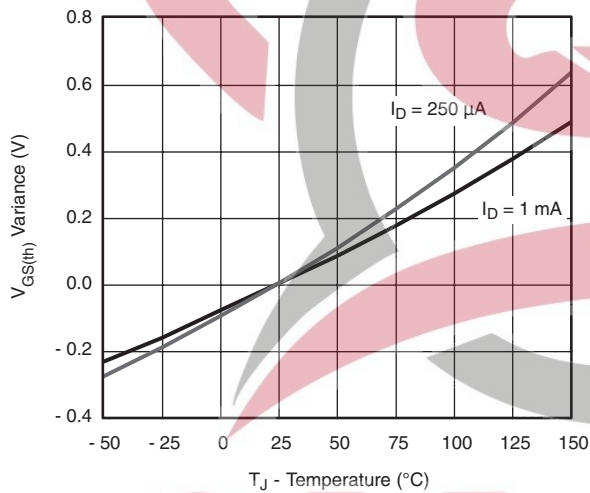
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



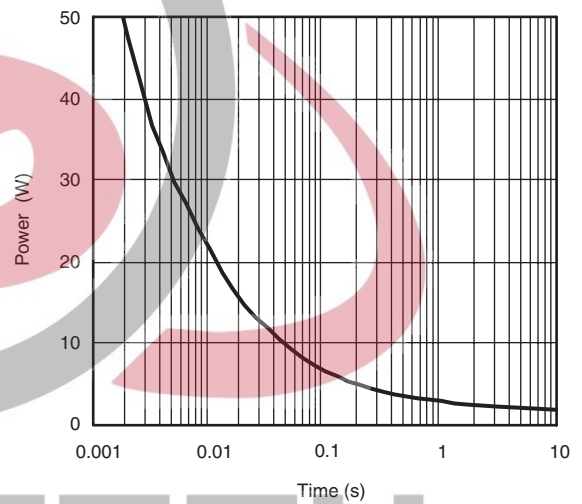
Source-Drain Diode Forward Voltage



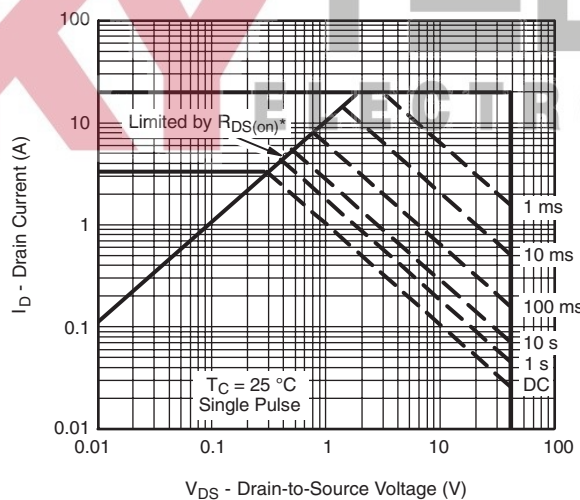
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



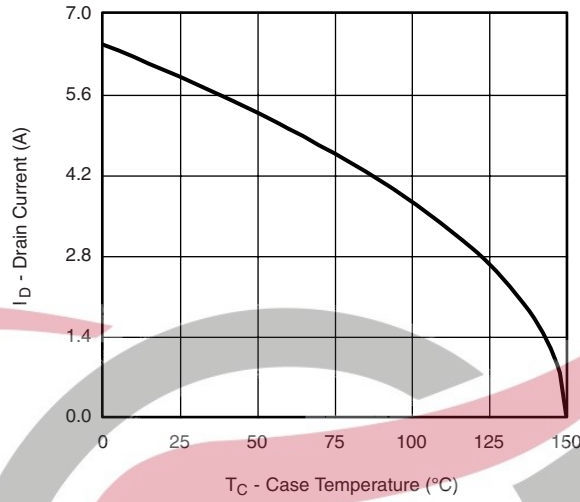
Single Pulse Power, Junction-to-Ambient



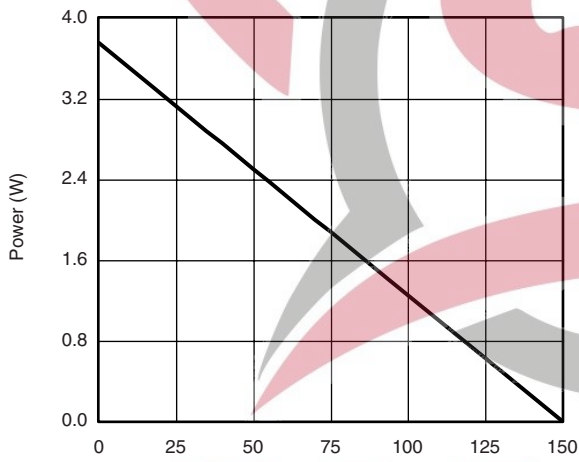
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

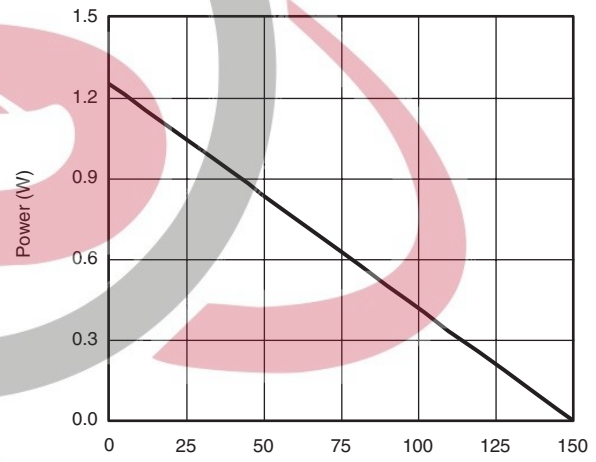
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



T_C - Case Temperature (°C)
Power Derating, Junction-to-Foot

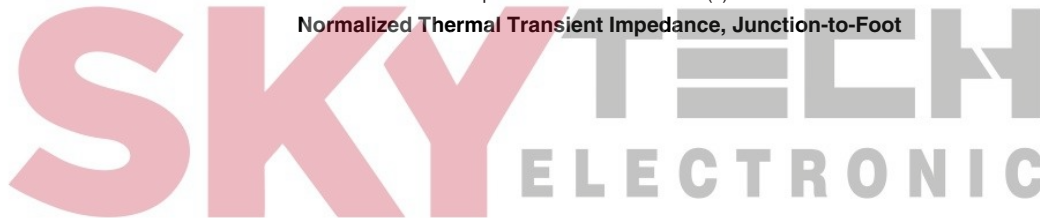
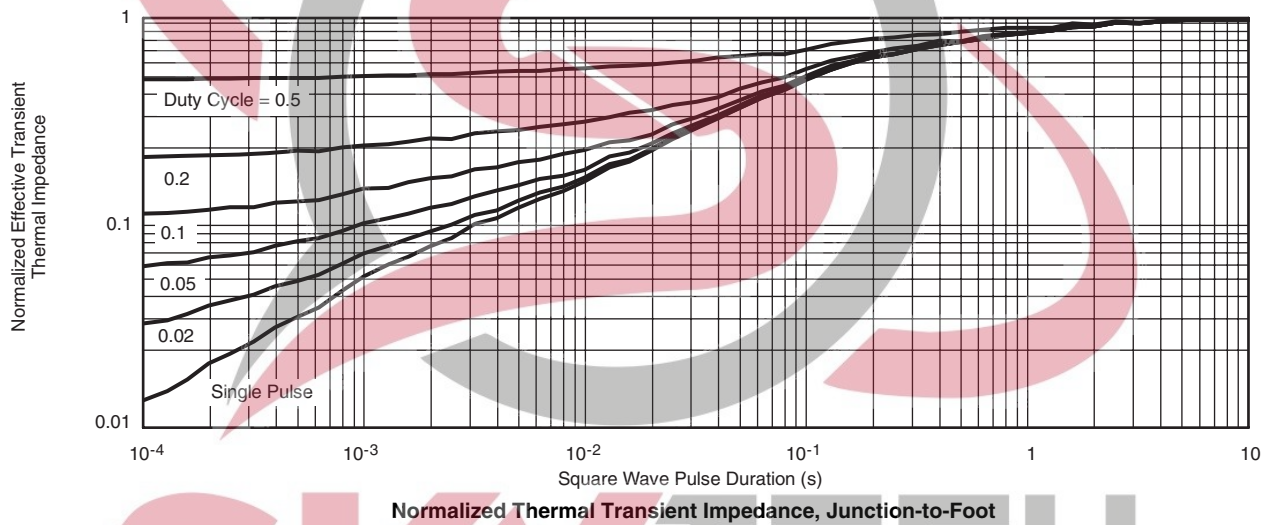
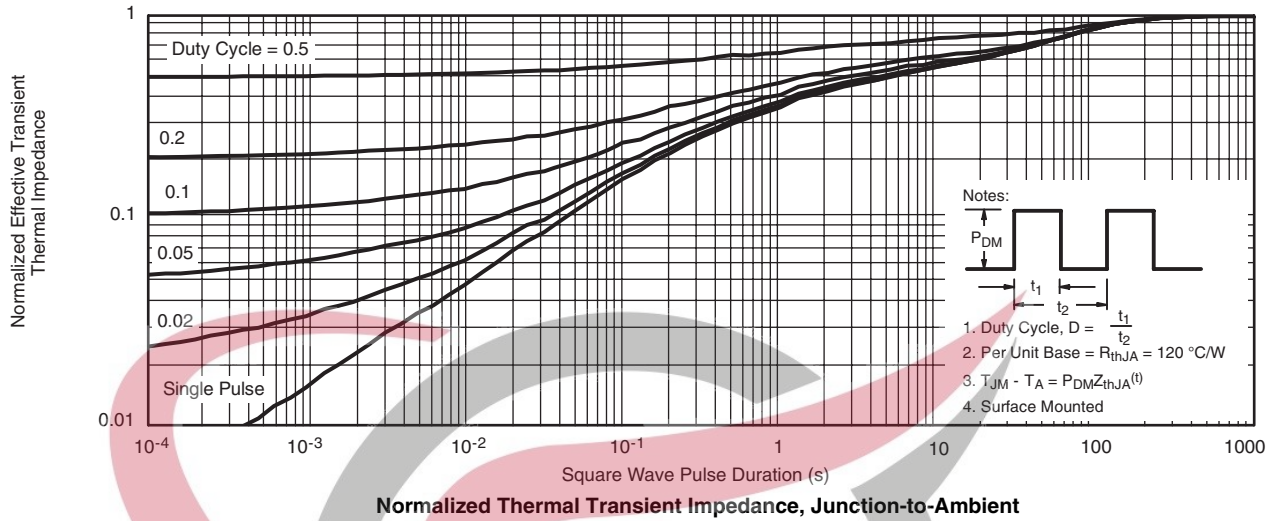


T_A - Ambient Temperature (°C)
Power Derating, Junction-to-Ambient



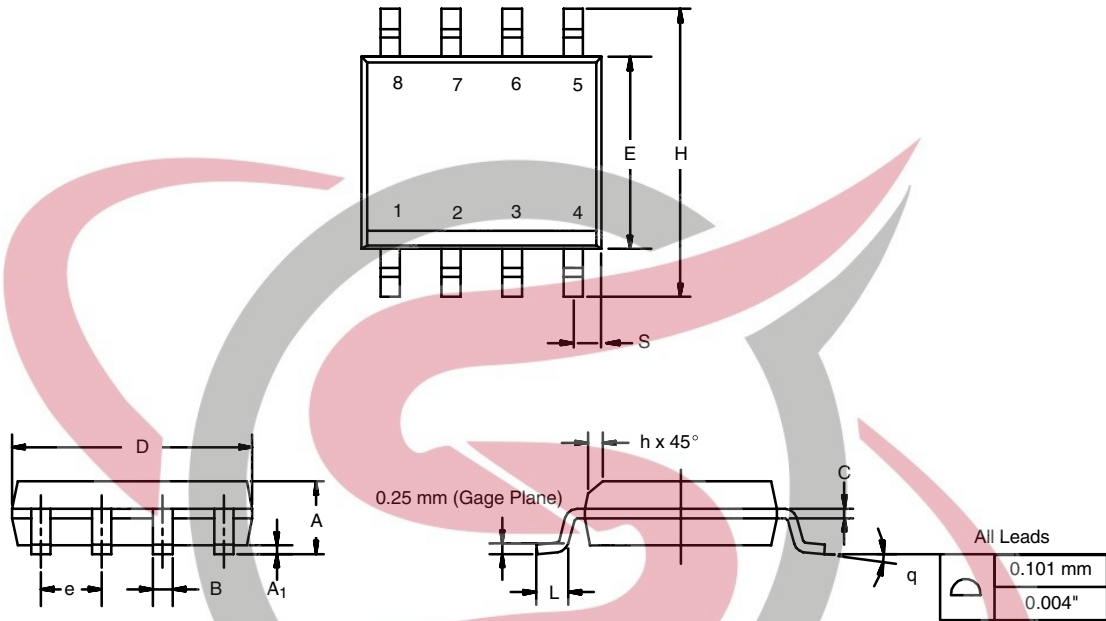
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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



SOIC (NARROW): 8-LEAD

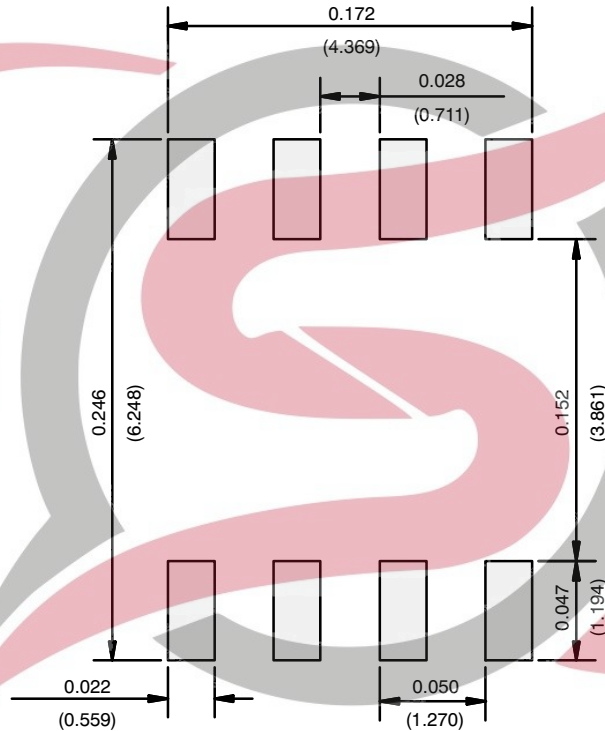
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Din-Tek documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Din-Tek documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.